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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,610	06/26/2003	Frank C. Wirtz II	X-1125 US	4919

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EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No.	Applicant(s)	
	10/606,610	WIRTZ ET AL.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26,28-38 and 40-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *26,28-38,40-44 and 52* is/are allowed.

6)☒ Claim(s) *1,2,6,7,15,19,20,24 and 45-48* is/are rejected.

7)☒ Claim(s) *3-5,8-14,16-18,21-23,25 and 49-51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 15, 19 and 45-48 are rejected under 35 U.S.C. 102(b) as being anticipated by Ong et al. (US PAT No. 5,821,772).

Regarding claim 1, Fig. 2 of Ong et al. teaches an integrated circuit comprising: a configurable function unit (21, Counter is designed, i.e. configured not to provide the count 00000; col. 3, lines 6-10) including a configurable function unit component (a counter is inherently comprised of configurable function units, e.g. logic gates); and at least one configurable decoder (DEC0 - DEC15 are programmed or configured by BITSTREAM1) having decoder configuration data (data in A0-1 - A0-5 in DEC0) and a decoder output (output of AND00), the configurable decoder being operable to decode a value in data presented by the configurable function unit component (output data presented by counter 21); wherein the configurable decoder is optimized to assert the decoder output based on a comparison of the decoder configuration data with the value presented by the configurable function unit component (decoder 21 is optimized to provide loading the data in different order; col. 3, lines 25-37).

Regarding claim 2, Fig. 2 of Ong et al. teaches the integrated circuit of claim 1, wherein the decoder configuration data is specified by configuring decoder cells having cell values of binary logic one, and binary logic zero, (address memory cells A0-1 - A0-5 are filled with binary logic one and/or zero respectively) and wherein the decoder output is asserted when the value presented by the configurable function unit component are consistent with the cell values (XNOR gates X0-1 - X0-5 perform comparison and provides output when data are matched, i.e. consistent with counter output).

Regarding claim 15, Fig. 2 of Ong et al. teaches the integrated circuit of claim 1, where the configurable function unit component is a counter (21 is counter).

Regarding claim 19, Fig. 2 of Ong et al. teaches the integrated circuit of claim 15 where the decoder output is synchronized and provided to the logical interconnect network (when the counter 21 provides the count that is the same as the address memory cells A0-5 through A0-1, AND gate AND00 provides high signal to the address line A0, i.e. the output of the decoder is synchronized).

Regarding claim 45, Fig. 2 of Ong et al. teaches a CPLD having interconnectable programmable logic (FPGA has logic blocks configured by memory cells; col. 1, lines 15-20), configuration memory (M0-0 - M15-15), and external inputs and outputs (external inputs and outputs are inherent in a FPGA to communicate with other devices), the interconnectable programmable logic being connected by a logical

interconnection matrix (FPGA has routing configured by memory cells; col. 1, lines 15-20), and the CPLD comprising: a configurable function unit (21, Counter is designed, i.e. configured not to provide the count 00000; col. 3, lines 6-10) including a configurable function unit component (a counter is inherently comprised of configurable function units, e.g. logic gates); and a configurable decoder (DEC0 - DEC15 are programmed or configured by BITSTREAM1) operable to assert a decoder output upon detecting a decode value in data presented by the configurable function unit component (decoder 21 is optimized to provide loading the data in different order; col. 3, lines 25-37).

Regarding claim 46, Fig. 2 of Ong et al. teaches the CPLD of claim 45, wherein a decoder configuration associated with the configurable decoder comprises decoder cells, which are configured to match output bits of the configurable function unit component corresponding to binary logic one, binary logic zero, (address memory cells A0-1 - A0-5 are filled with binary logic one and/or zero respectively) and corresponding to a value that matches either binary logic one, binary logic zero, or that matches both binary logic one and binary logic zero (XNOR gates X0-1 - X0-5 perform comparison and provides output when data are matched, i.e. consistent with counter output).

Regarding claim 47, Fig. 2 of Ong et al. teaches the CPLD of claim 45 where the configurable function unit is logically internal to a predetermined function block of the CPLD (the counter 21 is within a decoder structure (predetermined function) having a programmable address decoder with a counter).

Regarding claim 48, Fig. 2 of Ong et al. teaches the CPLD of claim 45 where the configurable function unit is logically internal to a predetermined specialized macrocell logically within the predetermined function block (the counter 21 is within a decoder structure (predetermined specialized macrocell) having a programmable address decoder with a counter).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ong et al. in view of New (US PAT No. 6,288,570).

Regarding claims 6, 36 and 43, Fig. 2 of Ong et al. teaches the integrated circuit of claims 1, 26 and 38 as discussed above where the FPGA includes logic blocks, but does not teach the integrated circuit is an FPGA including at least one look-up table. However, Fig. 12a of New discloses a configurable logic blocks including at least one look-up table (J, H, G, F) for the purpose of providing simple implementation of any one of logic functions (col. 7, lines 25-26, col. 13, lines 55-56). Therefore, it would have been at the time the invention was made to a person ordinary skilled in art to implement the look-up table of New in the logic block of Ong et al. to simplify implementation of a logic function.

Regarding claim 7, Fig. 2 of Ong et al. teaches the integrated circuit of claim 1, as discussed above where the FPGA is a complex programmable logic device (FPGA is complex device compared to a logic gate) including logic blocks, but does not teach the logic blocks including a plurality of macrocells. However, Fig. 12a of New discloses a configurable logic blocks including look-up tables (each look-up table, J, H, G, F performs a macrofunction, i.e. a macrocell) for the purpose of providing simple implementation of any one of logic functions (col. 7, lines 25-26, col. 13, lines 55-56). Therefore, it would have been at the time the invention was made to a person ordinary skilled in art to implement the look-up tables of New in the logic block of Ong et al. to simplify implementation of a logic function.

Claims 20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ong et al. in view of Higashitsutsumi (US PAT No. 5,226,063).

Regarding claims 20 and 24, Fig. 2 of Ong et al. teaches the integrated circuit of claim 1 where the configurable function unit component is a counter designed not provide the count 0000 (col. 3, lines 6-10), but does not disclose the counter is a shift register or a feedback shift register. However, Fig. 5 of Higashitsutsumi teaches a counter comprising of shift registers (15a, 15b, 15c, 15d) with a feedback from the output of 15d and 15a to the input of 15a via an exclusive NOR gate for the purpose of providing a polynominal function where the polynomial function prevents the count 0000. Therefore it would have been obvious at the time the invention was made to a

person ordinary skill in the art to utilize the polynominal counter (counter with no 0000 count) having shift registers with feedback of Higashisutsumi in place of the counter of Ong et al. since it would provide a polynominal function (count with no 0000 count).

Allowable Subject Matter

Claims 26, 28-38, 40-44 and 52 is allowable over the prior art of record.

Claims 3-5, 8-14, 16-18, 21-23, 25, and 49-51 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The indication of the allowable subject matters has been discussed in the previous Office action.

Response to Arguments

Applicant's arguments filed March 8, 2005 have been fully considered but they are not persuasive.

The applicant asserts that Ong's counter is not shown to be configurable and does not suggest the claimed configurable function unit. The examiner notes that the counter 21 of Ong clearly teaches that it is designed, i.e. configured, not provide the count 00000 as discussed in col. 3, lines 6-10. Therefore, Ong's counter is configurable to be set not to count an user configured count. The examiner notes that Ong's counter provides a fixed counting function once the counter has been configured. The applicant also argue that Ong's decoder are not shown to be configurable and do not suggest the claimed configurable decoders. The examiner notes that Ong's decoder includes XNOR

gates, AND gates, and address memory cells provides a programmable decoder function as discussed on col. 2, line 60 - col. 3, line 24) where the counter 21 provides the counts. The decoder is programmable, i.e. configurable since the data in the address memory cells is configurable by an user, which determines the output of the decoder. The applicant further argues that claim 2 is not being anticipated by Ong because the data input to Ong's decoder does not configure the function of the decoders. The examiner notes that the decoder is a programmable/configurable by the data in the address memory cells, i.e. the different address data is inputted in the address memory cells so that the decoder is configured to output a corresponding counter output data. Therefore, Ong's programmable address decoder teaches all limitation recited in claim 2.

In response to applicant's argument that there is no suggestion to combine the references over claims 6-7, 20, 24, 36-37 and 43-44, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, New (US PAT No. 6,288,570) teaches a look-up table in a FPGA provides a simplified logic function as recited in claim 6, which is considered to be obvious to a person ordinary skill in the art to be implemented in a FPGA. As for claims 7, 37 and 44, the applicant argues that Ong or New do not suggest a

CPLD(complex programmable logic device). The examiner notes that the structure of FPGA of Ong or New is a complex programmable logic device compared to a simple AND gate with a programmable cell. The examiner further notes that claims 7, 37, and 44 has no structural limitation distinguishing from FPGA of Ong or New other than a plain language of being a complex programmable logic device. As for claims 20 and 24, the applicant argues that there was no proper motivation in combining Ong reference with Higahitsutsumi. The examiner notes that the counter of Ong has the counter function with no 0000 count, but does not show the details of the counter having no 0000 count. However, the polynomial counter of Higashisutsumi provides the details of a counter having no 0000 count for the purpose of providing a polynomial function, i.e. having no 0000 count. The polynomial counter of Higahitsutsumi counts 1-15 in decimal prohibiting the count of 0000 in binary. The applicant further argues that combining Higahitsutsumi with Ong would make Ong nonfunctional. The examiner notes that the counter of Higahitsutsumi provides a counter with no 0000 count having shift register would fit for the function of Ong which is designed not to provide 0000 count.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James Cho
Primary Examiner
Art Unit 2819

May 23, 2005